

7/12/03

RECEIVED

JUL 11 2003

Technology Center 2100

DECLARATION FOR TRANSLATION

I, Jun Ishida, a Patent Attorney, of 1-34-12, Kichijoji-Honcho, Musashino-shi, Tokyo, Japan, do solemnly and sincerely declare that I well understand the Japanese and English languages and that the attached English version is a full, true and faithful translation made by me

this 1st day of July 2003

of the Japanese priority document of

Japanese Patent Application
No. 2000-198164

entitled "SIGNAL PROCESSING CIRCUIT".

In testimony thereof, I herein set my name and seal

this 1st day of July 2003


Jun Ishida
Patent Attorney



RECEIVED

JUL 11 2003

Technology Center 2100

[Document] APPLICATION FOR PATENT

[Identification No. of Document] KJA1000025

[Filing Date] June 30, 2000

[Addressee] Esq. Commissioner of the Patent Office

[IPC] H03M 13/00

[Title of the Invention] SIGNAL PROCESSING CIRCUIT

[Number of Claims] 2

[Inventor]

[Address] c/o SANYO ELECTRIC CO., LTD. of 5-5, Keihan-Hondori 2-chome, Moriguchi-shi, Osaka, Japan

[Name] Naoyuki OGINO

[Applicant]

[Identification No. of Applicant] 000001889

[Name] SANYO ELECTRIC CO., LTD.

[Attorney]

[Identification No. of Attorney] 100075258

[Patent Attorney]

[Name] Kenji YOSHIDA

[Telephone No.] 0422-21-2340

[Assigned Attorney]

[Identification No. of Attorney] 100081503

[Patent Attorney]

[Name] Toshihiko KANAYAMA

[Telephone No.] 0422-21-2340

[Assigned Attorney]

[Identification No. of Attorney] 100096976

[Patent Attorney]

[Name] Jun ISHIDA

[Telephone No.] 0422-21-2340

[Official Fee]

[Registered No. for Payment] 001753

[Amount] ¥ 21,000

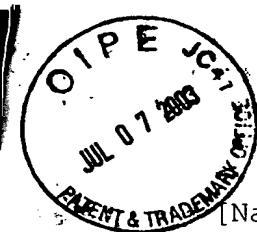
[List of Filing Papers]

[Name of Item] Specification
[Number] 1

[Name of Item] Drawings
[Number] 1

[Name of Item] Abstract
[Number] 1

[Necessity of Proof] Yes



[Name of Document]

Specification

RECEIVED

[Title of the Invention] SIGNAL PROCESSING CIRCUIT

JUL 11 2003

[Claims]

Technology Center 2100

1. A signal processing circuit for processing a signal reproduced
5 from a CD, comprising:

CDROM decoding means for decoding incoming CDROM data using a
memory; and

anti-shock controlling means for causing a predetermined amount
of incoming audio data to be stored in the memory, and reading and
10 outputting the audio data from the memory, so that continuous output
can be achieved even when the incoming audio data is interrupted, wherein
the CDROM decoding means and the anti-shock controlling means
use the same memory.

15 2. A signal processing circuit according to claim 1, further
comprising MP3 decoding means for performing MP3-decoding on
MP3-encoded data output from the CDROM decoding means.

[Detailed Explanation of the Invention]

20 [0001]

[Field of the Invention]

The present invention relates to a signal processing circuit
for use in a CD reproducing device for reproducing both CDROM data
and audio data.

25 [0002]

[Description of the Prior Art]

Portable CD players have become widely used as use of audio CDs has increased. Because the portable CD players are susceptible to external shocks which often result in reading errors, the players are usually provided with an anti-shock function.

5 [0003]

Meanwhile, MP3 (MPEG Audio Layer 3; MPEG stands for Moving Picture Experts Group) is gaining widespread use as an encoding format for audio data. MP3 data is utilized in such a manner that, for example, audio data MP3-encoded and compressed on a personal computer is exchanged 10 via the Internet or the like, and that users enjoy music obtained by decoding the data in real time on a personal computer.

[0004]

However, with widespread use of CD-Rs and CD-RWs, users increasingly enjoy music using a player to play a CD in which MP3 data 15 is written as CDROM data, and therefore attempts to provide a portable CD player with a function of playing a CD with MP3 data written therein are beginning to be made.

[0005]

[Problems to be solved by the Invention]

20 The anti-shock function is performed by storing a predetermined amount of readout audio data in a memory and outputting the audio data read out from the memory so that audio data can be continuously output even when the incoming audio data is interrupted. Thus, a memory for storing audio data is required. Furthermore, when CDROM data read out 25 from a CD is decoded, a memory is required because it is necessary to temporarily store the data during the process. In this regard, when

an in-car CD system is provided with the anti-shock function, respective memories are required for the anti-shock function and CDROM decoding, as in the portable CDs.

[0006]

5 An object of the present invention is to provide a signal processing circuit capable of effectively using a memory.

[0007]

[Means for solving the Problems]

The present invention provides a signal processing circuit for 10 processing a signal reproduced from a CD, comprising CDROM decoding means for decoding incoming CDROM data using a memory, and anti-shock controlling means for causing a predetermined amount of incoming audio data to be stored in the memory, and reading and outputting the audio data from the memory, so that continuous output can be achieved even 15 when the incoming audio data is interrupted, wherein the CDROM decoding means and the anti-shock controlling means use the same memory.

[0008]

Thus, the use of a single memory can be shared as both memory for decoding the CDROM data and for the anti-shock function, thereby 20 allowing efficient use of the memory.

[0009]

Further, MP3 decoding means is preferably provided for performing 25 MP3-decoding on MP3-encoded data output from the CDROM decoding means, thereby allowing reproduction of both an audio CD and a CD with MP3 data.

[0010]

[Preferred Embodiments]

A preferred embodiment (hereinafter, referred to as an embodiment) of the present invention will next be described with reference to the drawings.

5 [0011]

Fig. 1 is a diagram illustrating a configuration of a signal processing circuit according to an embodiment. A signal read out from a CD is processed to digital data. CDROM data is supplied to a CDROM decoder 10, while CDDA data, which is audio data, is supplied to an 10 anti-shock controller 12. Such data identification is performed by an external microcomputer or the like based on the content of the readout signal, and the element to receive the data is determined based on the identified result.

[0012]

15 The CDROM decoder 10 decodes the data (digital data) read out from the CD, and outputs MP3-encoded data. During such a decoding process, the CDROM decoder 10 requires a memory for temporarily storing data for the sake of buffering the incoming data or checking and correcting errors. Therefore, the CDROM decoder 10 is connected to 20 an external memory 16 through an interface 14.

[0013]

Meanwhile, CDDA data is supplied to the anti-shock controller 12, which writes data in the external memory 16 through the interface 14 and sequentially outputs data read out from the external memory 25 16. When an error occurs in reading data from the CD due to external impact, the anti-shock controller 12 calculates and outputs the address

at the moment before the reading error occurs, and the data corresponding to the moment before the reading error occurs is read out from the external memory 16.

[0014]

5 The MP3-encoded data from the CDROM decoder 10 is supplied to an MP3 decoder 18, which issues a reading request to the CDROM decoder 10, receives the data read out from the external memory 16, and decompresses it to the original data. Through MP3 decoding, audio data similar to CDDA is obtained.

10 [0015]

The audio data from the MP3 decoder 18 and the audio data from the anti-shock controller 12 are supplied to a selection circuit (MUX) 20, which selects either one of the two.

[0016]

15 An output from the selection circuit 20 is supplied to a DAC (digital-to-analog converter) 22, which converts it to analog audio signals so that audio signals for reproduction are obtained.

[0017]

According to the present embodiment, the CDROM decoder 10, the
20 anti-shock controller 12, the interface 14, the MP3 decoder 18, and the selection circuit 20 are mounted on a one-chip LSI, to which an identification signal indicating whether the input data is CDROM data or CDDA data is supplied to control data processing and output.

[0018]

25 Fig. 2 is a diagram illustrating a configuration of the interface 14, and signal exchange with the CDROM decoder 10 and the anti-shock

controller 12.

[0019]

An identification signal CDROMO is externally supplied to the interface 14, the CDROM decoder 10, and the anti-shock controller 12.

5 The signal CDROMO is used to identify the incoming signal as either CDROM data or CDDA data.

[0020]

When the input data is CDROM data, the signal CDROMO enables the CDROM decoder. The CDROM decoder initiates a process for decoding

10 the incoming CDROM data, and supplies a request signal Req to the interface 14 when data writing becomes necessary. The request signal

Req is supplied to an arbiter 142 for CDROMs provided in the interface 14. The CDROM arbiter 142 is also supplied with a signal regarding refresh timing of the external memory (DRAM) 16 from a refresh counter

15 144 provided in the interface 14, and supplies a control signal for writing to a selection circuit 150 at writable timing. Furthermore,

the CDROM decoder 10 supplies write data to the external memory 16 through a data input unit 146 provided in the interface 14. The write

address is supplied to an access control unit 148 in the interface

20 14 from the CDROM decoder 10.

[0021]

An arbiter 152 for the anti-shock controller is also provided for the selection circuit (multiplexer: MUX) 150. The selection circuit

150 is supplied with the identification signal CDROMO, and supplies

25 a control signal for memory access supplied from the CDROM arbiter 142 to the access control unit 148 for the selection circuit 150 when

CDROM data is input.

[0022]

Thus, RAS and CAS signals necessary for matrix access to the external memory 16, which is DRAM, and Address and Write Enable (WE) 5 signals necessary for access to the external memory 16 are output from the access control unit 148. Consequently, data supplied from the CDROM decoder 14 to the external memory 16 through the data input/output unit 146 is written in a specified address.

[0023]

10 When a need for data readout from the external memory 16 arises in the CDROM decoder 10, the CDROM decoder 10 supplies a readout request signal to the CDROM arbiter 142, which supplies a control signal to the access control unit 148 through the selection circuit 150 at predetermined timing. It should be noted that the CDROM decoder 10 15 outputs a plurality of request signals for reading/writing data, such as CDROM data, subcode signals, error flags for error correction, and the like, or for processing such data for other purposes. The CDROM arbiter 142 outputs a plurality of control signals in the order of priority in accordance with such request signals or a readout request 20 (not shown) received from the MP3 decoder 18. The access control unit 148 supplies an output enable signal OE, and RAS, CAS, and Address signals to the external memory 16, and data at the address is captured into the CDROM decoder 10 through the data input/output unit 146.

[0024]

25 When CDDA data is input, the anti-shock controller 12 assumes an operation enable state in accordance with the identification signal

CDROMO. For an access to the external memory 16, the request signal Req is supplied from the controller 12 to the anti-shock controller arbiter 152, and the selection circuit 150 selects the anti-shock controller arbiter 152 in accordance with the identification signal

5 CDROMO. A control signal is supplied from the anti-shock controller arbiter 152 to the access control unit 148 through the selection circuit 150. It should be noted that the anti-shock controller 12 outputs a plurality of request signals for reading and writing data, such as CDDA data, subcode signals, error flags, and the like, or for processing

10 such data for other purposes. The anti-shock controller arbiter 152 outputs a plurality of control signals corresponding to the request signals. The write enable signal WE and the output enable signal OE are supplied to the external memory 16 for writing and reading, respectively. The anti-shock controller 12 supplies write data to the

15 external memory 16 through the data input/output unit for writing, and captures data from the external memory 16 through the data input/output unit 146 for reading. Thus, input data from the anti-shock controller 12 can be written into the external memory 16, and data written in the external memory 16 can be read out.

20 [0025]

As described above, according to the present embodiment, the external memory 16, which is a single memory, can be utilized as a memory for use in both reading and writing of CDROM data necessary for the CDROM decoder 10, and in reading and writing of CDDA data for

25 the anti-shock controller 12.

[0026]

The external memory 16 is addressed by dividing the external memory 16 into two memory areas so that CDDA data and CDROM data are written in the respective areas. The external memory 16 is more preferably treated as a single memory area. More specifically, for 5 CDDA reproduction, the CDDA data is written into and read from approximately the entire memory area of the external memory 16, while for MP3 reproduction, CDROM data is written into and read from approximately the entire memory area of the external memory 16. Upon switching between CDDA reproduction and MP3, data remaining in the 10 external memory 16 is overwritten with new data, thereby rewriting data therein. Thus, the external memory 16 can be efficiently utilized, and audio data for the period of time corresponding to the capacity of the external memory 16 can be stored. As a result, the anti-shock function can be improved because the player can be resistant to impact 15 for a longer period of time, and a greater amount of data can be used for MP3 decompression, leading to higher decompression efficiency.

[0027]

Thus, only a single memory is sufficient as memory to be connected to an LSI, resulting in reduction in number of external memories, and 20 therefore enabling reduction in number of terminals of the LSI and simplification of circuitry. Because either an MP3-formatted CD or a CDDA-formatted CD is employed, the input data is in either one of these formats, and therefore the external memory 16 can be shared for these purposes without problems.

25 [0028]

Further, audio output can be achieved during replay of either

one of a CD with MP3-compressed data stored or a CD with CDDA data stored. The present invention is applicable not only in MP3 techniques but also in other compression/decompression techniques.

[0029]

5 [Advantages]

As described above, according to the present invention, a single memory can be shared as memory for use both in decoding of CDROM data and in an anti-shock function, thereby enabling effective use of a memory.

10 [Brief Description of the Drawings]

[Fig. 1] A diagram illustrating a configuration of a signal processing circuit according to an embodiment.

[Fig. 2] A diagram illustrating a configuration of an interface circuit.

15 [Explanation of Reference Numerals]

10 CDROM DECODER

12 ANTI-SHOCK CONTROLLER

14 INTERFACE

16 EXTERNAL MEMORY

20 18 MP3 DECODER

20 SELECTION CIRCUIT

[Name of Document] Abstract of the Disclosure

[Summary]

[Problems] To effectively use a memory.

[Structure] An external memory 16 is accessed by either a CDROM decoder
5 10 or an anti-shock controller 12 through an interface. Thus, a single
memory can be shared for two purposes, allowing both audio data and
MP3 data to be reproduced in an efficient manner.

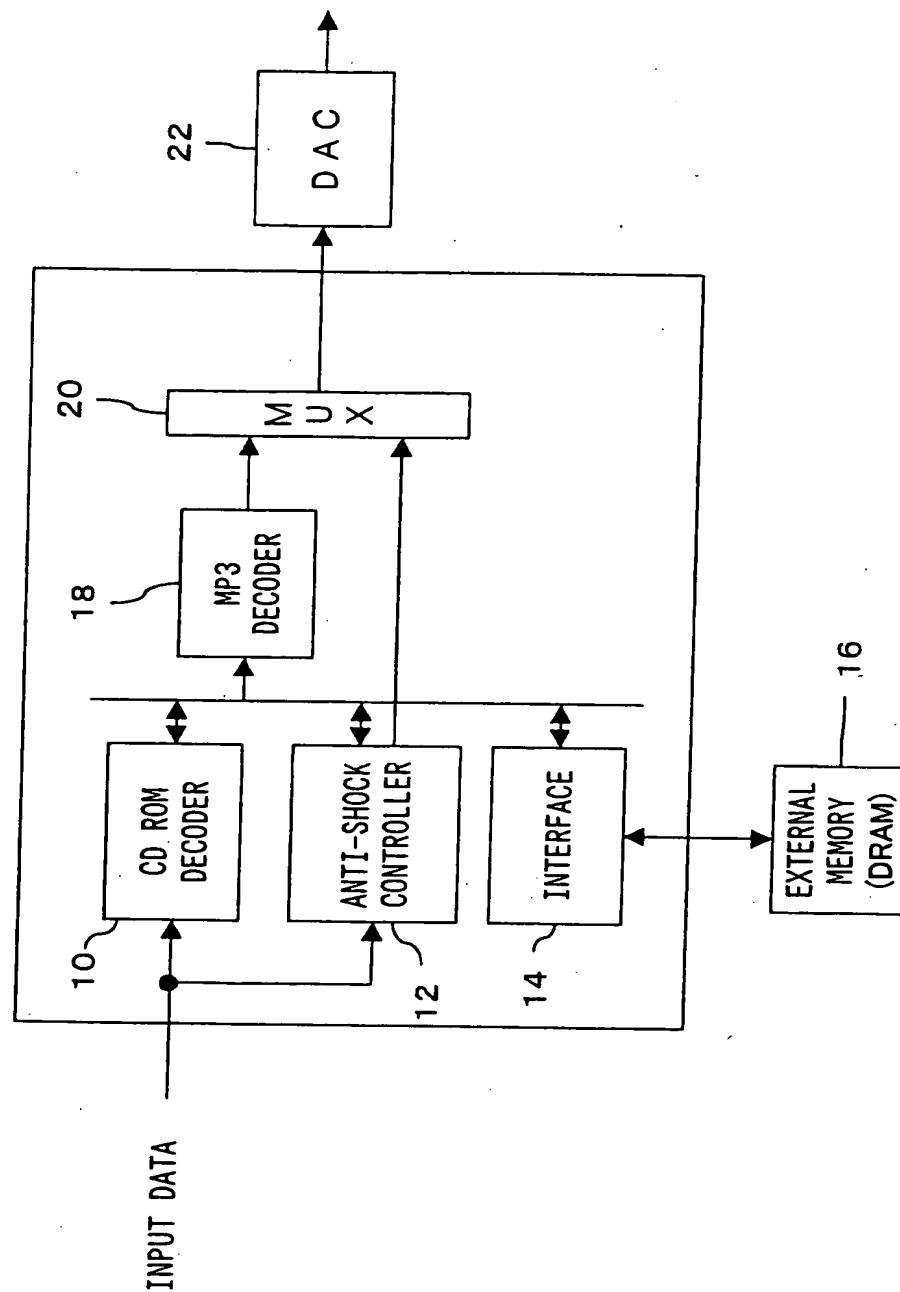
[Selected Drawing] Fig. 1

10



[Name of Document] Drawings

[Fig. 1]





[Fig. 2]

